In the Claims:

1.-32. (Canceled)

33. (Original) A method of fabricating a transistor, the method comprising:

providing a workpiece, the workpiece having a top surface;

implanting germanium into the top surface of the workpiece, forming an amorphous germanium-containing region within the top surface of the workpiece, the amorphous germanium-containing region extending about 45 Å or less beneath the workpiece top surface, wherein implanting germanium into the top surface of the workpiece also forms a first crystalline germanium-containing region beneath the amorphous germanium-containing region, the first crystalline germanium-containing region extending about 55 Å or less beneath the amorphous germanium-containing region;

depositing a gate dielectric material over the amorphous germanium-containing region, the gate dielectric material having a dielectric constant of about 4.0 or greater;

annealing the workpiece at a temperature of about 750 °C or less for about 60 minutes or less, re-crystallizing the amorphous germanium-containing region and forming a single second crystalline germanium-containing region within the top surface of the workpiece, the single second crystalline germanium-containing region comprising the re-crystallized amorphous germanium-containing region and the first crystalline germanium-containing region, the second crystalline germanium-containing region extending about 120 Å or less beneath the workpiece top surface;

depositing a gate material over the gate dielectric material;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric over the second crystalline germanium-containing region; and

forming a source region and a drain region in at least the second crystalline germanium-containing region.

34. (Original) The method according to Claim 33, wherein implanting the germanium into the top surface of the workpiece comprises forming a damage region between first germanium-containing region and the second germanium-containing region, further comprising annealing the workpiece, converting the amorphous germanium-containing region to a second crystalline germanium-containing region, the first crystalline germanium-containing region and the second crystalline germanium-containing region comprising a single crystalline germanium-containing region, and wherein annealing the workpiece causes the removal of the damaged region between the first germanium-containing region and the second germanium-containing region.

35. (Original) The method according to Claim 33, wherein implanting the germanium comprises implanting germanium at an energy dose of about 5 keV or less and at a dose of about 1×10^{15} to 1×10^{17} atoms/cm^2.

36. (Original) The method according to Claim 33, wherein implanting the germanium comprises forming the first germanium-containing region comprising at least 50% germanium at a top portion thereof.

37. (Original) The method according to Claim 33, wherein the depositing the gate dielectric material comprises depositing HfO_2, $HfSiO_X$, Al_2O_3, ZrO_2, $ZrSiO_X$, Ta_2O_5, La_2O_3, Si_xN_y, SiON, or combinations thereof.

38. (Original) The method according to Claim 33, wherein forming the source and drain regions comprises a temperature of about 938.3 °C or less.